Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 7. A fabrication method for a split gate flash memory cell, comprising:
providing a substrate;
forming a stack structure on the substrate, wherein the stack structure is formed with, sequentially from the substrate, a tunneling dielectric layer, a floating gate and a cap layer;
forming a source region in the substrate beside a first side of the stack structure;
forming inter-gate dielectric layers on sidewalls of the stack structure;
forming a trench in the substrate beside a second side of the stack structure;
forming a selective gate dielectric layer at a bottom and on a sidewall of the trench;
forming a selective gate on the sidewall at the second side of the stack structure and on the sidewall of the trench; and
forming a drain region at the bottom of the trench beside a side of the selective gate.

[c2] 8. The method of claim 7, wherein the step of forming

the selective gate on the sidewall at the second side of the stack structure and the sidewall of the trench comprises:

forming a conductive layer on the substrate; and

removing a portion of the conductive layer to form a conductive spacer on the sidewall at the first side of the stack structure, and the selective gate on the sidewall at the second side of the stack structure and the sidewall of the trench.

[c3] 9. The method of claim 8, wherein the step of removing the portion of the conductive layer comprises performing an anisotropic etching method.

[c4] 10. The method of claim 8, wherein after forming the selective gate on the sidewall at the second side of the stack structure and the sidewall of the trench further comprises a step of removing the conductive spacer.

[c5] 11. The method of claim 7, wherein the step of forming the inter-gate dielectric layers on the sidewalls of the stack structure comprises:

forming a silicon oxide layer on the sidewall of the floating gate; and

forming a silicon nitride layer on the silicon oxide layer.

[c6] 12. The method of claim 7, wherein the steps of forming

the inter-gate dielectric layer at the bottom and on the sidewall of the trench comprises performing a thermal oxidation method.

[c7] 13. A fabrication method for a split gate flash memory device, comprising:
providing a substrate;
forming a tunneling dielectric layer, a first conductive layer and a mask layer sequentially on a substrate;
patterning the mask layer to form an opening that exposes a portion of the first conductive layer;
forming a cap layer on the exposed first conductive layer;
removing the mask layer;
etching the first conductive layer and the tunneling dielectric layer to form a stack structure, using the cap layer as a mask;
forming a source region in the substrate beside a first side of the stack structure;
forming inter-gate dielectric layers on sidewalls of the stack structure;
forming a trench in the substrate beside a second side of the stack structure;
forming a selective gate dielectric layer on a sidewall and at a bottom of the trench;
forming a second conductive layer on the substrate;

removing a portion of the second conductive layer to form a conductive spacer on the sidewall at the first side of the stack structure, and a selective gate on the sidewall at the second side of the stack structure and on the sidewall of the trench; and
forming a drain region at the bottom of the trench beside a side of the selective gate.

[c8] 14. The method of claim 13, wherein the step of removing the portion of the second conductive layer includes anistropic etching.

[c9] 15. The method of claim 13, wherein after the steps of removing the portion of the second conductive layer to form the conductive spacer on the sidewall at the first side of the stack structure, and the selective gate on the sidewall at the second side of the stack structure and on the sidewall of the trench, and forming the drain region at the bottom of the trench at the one side of the selective gate, the method further comprises a step of removing the conductive spacer.

[c10] 16. The method of claim 13, wherein the step of forming the inter-gate dielectric layers on the sidewalls of the stack structure comprises:
forming a silicon oxide layer on a sidewall of the floating gate; and

forming a silicon nitride on the silicon oxide layer.

[c11] 17. The method of claim 13, the selective gate dielectric layer on the sidewall and at the bottom the trench is formed by a thermal oxidation method.

[c12] 18. The method of claim 13, wherein the step of forming the cap layer on the exposed first conductive layer comprises performing thermal oxidation.